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**B. TECH-II SEM-I II-MIDEXAMINATIONS**

**SET-II**

**Date:03/12/24 Time:10:00Am**

**Subject: COA Branch: IT**

**PART-A 5x 2M =10 M**

**BTL CO**

1. List out the modes of Transfer **1 4**
2. Difference between Main memory and Secondary memory **5 4**
3. Difference between Hand shaking and Strobe **5 4**
4. Define Pipelining with examples **5 5**
5. Explain instruction pipeline **2 5**

**PART-B 4 x 5 M = 20 M**

**BTL CO**

1. Discuss Multiplication using Booth’s Algorithm with example? **2 3**
2. Explain about I/O Interface with neat diagram? 2 4
3. Explain about associate memory with neat diagram ? 2 4
4. Discuss the CISC & RISC architecture with neat diagram **5 5**
5. Explain about Arithmetic pipeline with flow chart ? **2 5**
6. Explain about Cache coherence problem with neat diagram 2 5

**SCHEME OF EVALUATION**

**Part –A**

| **SNO** | **THEORY** | **MARKS** | **TOTAL** |
| --- | --- | --- | --- |
| **1** | modes of Transfer | **2** | **2** |
| **2** | Difference between Main memory and Secondary memory | **2** | **2** |
| **3** | Difference between Hand shaking and Strobe | **2** | **2** |
| **4** | Define Pipelining with examples | **2** | **2** |
| **5** | Explain instruction pipeline | **2** | **2** |

**Part –B**

| **SNO** | **THEORY** | **MARKS** | **TOTAL** |
| --- | --- | --- | --- |
| **6** | Multiplication using Booth’s Algorithm with example | **5** | **5** |
| **7** | I/O Interface with neat diagram | **5** | **5** |
| **8** | associate memory with neat diagram. | **5** | **5** |
| **9** | CISC & RISC architecture with neat diagram | **5** | **5** |
| **10** | Arithmetic pipeline with flow chart | **5** | **5** |
| **11** | Cache coherence problem with neat diagram | **5** | **5** |